PIPELINED MULTIPLY-ACCUMULATE UNIT AND OUT-OF-ORDER COMPLETION LOGIC FOR A SUPERSCALAR DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

A mechanism for, and method of, processing multiply-accumulate instructions with out-of-order completion in a pipeline, for use in a processor having an at least four-wide instruction issue architecture, and a digital signal processor (DSP) incorporating the mechanism or the method. In one embodiment, the mechanism including: (1) a multiply-accumulate unit (MAC) having an initial multiply stage and a subsequent accumulate stage and (2) out-of-order completion logic, associated with the MAC, that causes interim results produced by the multiply stage to be stored when the accumulate stage is unavailable and allows younger instructions to complete before the multiply-accumulate instructions.